REMARKS

Summary of Office Action

Claims 8-13 are pending in the application.

Claims 8-13 have been rejected under 35 U.S.C. § 101 as failing the "useful, concrete, and tangible result" criteria. Claims 18-13 also have been rejected under 35 U.S.C. 102(b) as being anticipated by Pechanek et al. U.S. Patent No. 6,101,592 ("Pechanek").

The Examiner has noted and objected to informalities in specification and the claims.

Applicants' Reply

Applicants have amended the specification and the claims to correct the informalities that were kindly noted by the Examiner.

Applicants have amended claims 8, 10-13 for clarity. claim 9 is canceled and its limitations included in claim 8.

Applicants respectfully traverse the § 101 rejections and the § 102 rejections.

§101 rejections

Applicants invention improves on the VLIW code architecture density in the TVLIW scheme.

By means of TVLIW, an actual VLIW is assembled out of a limited number of TVLIW containers. Each function instruction word FIW is executed in one function unit FU. Therefore each TVLIW container (i.e. a part of the TVLIW) includes a FIW and a tag indicating the 'owning' FU. A decoder is used to decode the TVLIW codes and sends the resulted VLIW codes to the processor core. (See specification, Background of the Invention).

Applicants have found that there is a non-uniform distribution for these tag combinations or FU combinations. This means instructions with some FU combinations are much more used than others. Applicants' invention exploits the frequency distribution of FU combinations to reduce the code size by creating a HVLIW. In particular, the invention compresses the most used FU combinations to reduce the code size. After generation a HVLIW is executed instead of a TVLIW. (See e.g. specification, Summary of the Invention)

Applicants have amended claim 8 to explicitly include the step of "executing the HVLIW with its code-compressed structure to actuate the functioning units (FUs) in the processor." No new matter is added. (See e.g., Specification ¶[0025]).

Applicants submit that the method of claim 8 is practical, and has the useful, tangible and concrete result of actuating functional units of processor as desired in the preamble.

Applicants submit that claims 8, and 9-13 conform to all requirements of § 101

§102 rejections

Applicants note the method of claim 8 requires conversion of a TVLIW into HVLIW with a general header that includes FU-combination information on which of the FIWs is to be used for actuating a respective FU in the processor after decoding.

Penachek describes an hierarchical instructional set architecture (ISA). Penachek does not describe conversion of a TVLIW into HVLIW with a general header that includes FU-combination information on which of the FIWs is to be used for actuating a respective FU in the processor after decoding, as is required by the method of claim 8.

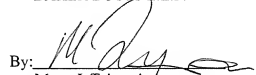
Accordingly, claim 8 is not anticipated by, and is patentable over Penachek. Further, dependent claims 10-13 are patentable over Penachek for at least the same reasons a parent claim 8.

Conclusion

In view of the foregoing remarks, favorable reconsideration and allowance of claims 8-13 are respectfully solicited. In the event that the application is not deemed in condition for allowance, the Examiner is invited to contact the undersigned in an effort to advance the prosecution of this application.

Respectfully submitted,

BAKER BOTTS L.L.P.

By: 

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